REMARKS

Applicants amend claims 1, 2, 4-6, 9-11, and 25 to more appropriately define the claimed subject matter and to correct informalities. Claims 1-25 are pending in this application, of which claims 13-24 are withdrawn from consideration.

Objection to Claim 2

The Examiner objected to claim 2 because of the following informalities: the last 2 lines of claim 2 recite the phrase "and the layers includes the patterns concurrently arranged each other." Claim 2 is being amended to delete this phrase. Thus, the amended claims are believed to overcome the Examiner's objection.

§ 102(e) Rejection of Claims 1-12 and 25 over *Kotani et al.* or *Yamauchi*

Applicants respectfully traverse the rejection of claims 1-12 and 25 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,853,743 to Kotani et al. ("*Kotani et al.*") or U.S. Patent Application Publication No. 2005/0034093 to Yamauchi ("*Yamauchi*"). To properly anticipate Applicants' claims under 35 U.S.C. § 102, each and every element as set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. "The identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). *See* MPEP § 2131, 8th Ed. (Rev. 5), August, 2007. *Kotani et al.* and *Yamauchi* fail to anticipate claims 1-12 and 25 because *Kotani et al.* and *Yamauchi* do not disclose each and every element of these claims.

Claims 1, 10, and 25 are not anticipated by *Kotani et al.* for at least the reason

that *Kotani et al.* fails to disclose a method comprising, inter alia, "extracting a first pattern of a first layer" and "extracting a second pattern of one or more second layers different from the first layer," as recited in amended independent claims 1, 10, and 25 (emphasis added).

Kotani et al. discloses "[a] mask pattern correction method used to form a desired pattern on a wafer by a projection optical system, comprising: a step of extracting a correction target edge from a design pattern; a step of calculating a length of the extracted correction target edge; a first step of calculating correction value determined one-dimensionally by pattern layout perpendicular to the correction target edge when the length of the correction target edge calculated in the previous step is not smaller than a predetermined critical length; and a second step of calculating correction value determined two-dimensionally by pattern layout around the correction target edge when the length of the correction target edge calculated in the previous step is smaller than a predetermined critical length" (claim 1).

However, *Kotani et al.* fails to disclose "extracting a first pattern of a first layer" and "extracting a second pattern of one or more second layers different from the first layer," as required by amended claims 1, 10, and 25. Extracting a target edge from a single design pattern, as disclosed by *Kotani et al.*, does not constitute "extracting a first pattern of a first layer" and "extracting a second pattern of one or more second layers different from the first layer," as recited in claims 1, 10, and 25 (emphasis added).

Moreover, *Kotani et al.* does not disclose "calculating a distance between the first and second patterns on a semiconductor substrate based on a predetermined process

variation," as required by claims 1 and 25 (emphasis added). For example, the calculation of *Kotani et al.* is not "based on a predetermined process variation." Rather, the correction value of *Kotani et al.* is calculated when the "target edge" is "smaller than a predetermined critical length" and "determined . . . by pattern layout" perpendicular to or around the target edge (claim 1 of *Kotani et al.*; emphasis added). *Kotani et al.* is silent on the matter of a "process variation," or on the matter of "calculating a distance between . . . patterns" based on "a predetermined process variation," as required by claims 1 and 25. Calculating a correction value based merely on a "pattern layout" around a target edge, as disclosed by *Kotani et al.*, does not constitute "calculating a distance between the first and second patterns . . . based on a predetermined process variation," as recited in claims 1 and 25, for at least the reason that the "pattern layout" of *Kotani et al.* does not constitute a "predetermined process variation."

Claims 1 and 25 are not anticipated by *Yamauchi* for at least the reason that *Yamauchi* fails to disclose "calculating a distance between the first and second patterns on a semiconductor substrate based on a predetermined process variation," as required by claims 1 and 25 (emphasis added).

Yamauchi discloses "[a] method for designing a semiconductor integrated circuit device," comprising "forming, on a substrate, a plurality of design patterns composed of circuit elements or wires, wherein a plurality of design rules having different values are applied to the plurality of design patterns by using dependence of respective finished sizes of the design patterns on a geometric feature of each of the design patterns" (claim 26).

However, applying design rules that merely use a geometric feature of each of the design patterns, as disclosed by *Yamauchi*, does not constitute "calculating a distance between the first and second patterns . . . based on a predetermined process variation," as required by claims 1 and 25 (emphasis added). For example, the "geometric features" of the design patterns of *Yamauchi* do not constitute a "predetermined process variation."

Claim 10 is not anticipated by *Yamauchi* for at least the reason that *Yamauchi* does not disclose "correcting the first design pattern in accordance with a correction rule of a design pattern that is defined by at least one of (i) widths of the first and second design patterns and (ii) a distance between the first and second design patterns" and "forming a mask pattern by further correcting, by process proximity effect correction, the first design pattern that has been corrected in accordance with the correction rule," as recited in amended claim 10 (emphasis added). Merely applying a design rule to a design pattern, as disclosed by *Yamauchi*, does not constitute "correcting [a] first design pattern in accordance with a correction rule" and then "further correcting . . . the [corrected] first design pattern" "by process proximity effect correction," as required by claim 10. Thus, *Yamauchi* fails to disclose each and every element of claim 10.

Since *Kotani et al.* and *Yamauchi* fail to disclose each and every element of independent claims 1, 10, and 25, these claims and claims 2-9, 11, and 12, which depend from claims 1 and 10, are not anticipated by *Kotani et al.* or *Yamauchi*.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to Deposit Account No. 06-0916.

Respectfully submitted,

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